Amendments to the Specification:

Please replace the paragraph beginning on pg. 4, line 4, with the following rewritten paragraph.

The problem of the "dishing effect" described above is particularly evident during the aforementioned method of forming shallow isolation regions. In addition to the deformation of the polishing pad and the reaction of the slurry in recessed regions of the fill oxide, the "dishing effect" may be further augmented by "overpolishing" the polish stop layer. In particular, the surface of the polish stop layer may be "overpolished" or polished to a level spaced below the original upper surface of the polish stop layer to ensure that the fill oxide no longer resides above the polish stop layer. Furthermore, the "dishing effect" may be dependent on the pattern density of the topography. For example, a topography having relatively wide spaces between the isolation regions may include a large amount of nitride across the lateral portion of the topography, which typically results in a slower polish rate. Alternatively, topographies having relatively narrow spaces between isolation regions may include less nitride across the lateral surface of the semiconductor topography, typically resulting in a faster polish rate. Consequently. a thicker layer of nitride may be needed to compensate for the increase in the polish rate. In an embodiment that includes a varied pattern density (i.e., isolation regions spaced non-uniformly across a semiconductor substrate), portions of the topography with a large of amount of nitride may be etched at a different rate than the portions of the topography with a small amount of nitride. As such, a substantially non-planar surface may result and isolation regions of differing heights may be produced.

Please replace the paragraph beginning on pg. 7, line 1, with the following rewritten paragraph.

A method for fabricating shallow trench isolation regions is also provided herein. Such a method may include forming one or more trenches extending through a stack of at least three layers arranged over a semiconductor substrate. Such a stack of layers may be formed in a single process chamber or one or more different process chambers prior to the formation of the trenches. The method may further include blanket depositing a dielectric over the trenches and the stack of layers such that the trenches are filled by the dielectric. The dielectric may then be planarized such that upper surfaces of the dielectric remaining within the trenches are coplanar with an upper surface of an adjacent layer of the stack. In addition, the method may include etching the upper surface of the adjacent layer to expose the semiconductor substrate. In some embodiments, upper portions of the dielectric may extend less than approximately 500 angstroms above the upper surface of the semiconductor substrate subsequent to etching the upper surface. More

specifically, the upper portions of the dielectric may extend between approximately 300 angstroms and approximately 500 angstroms above the upper surface of the semiconductor substrate subsequent to etching the upper surface. In either embodiment, the average thicknesses of the upper portions of the dielectric layer extending above the semiconductor substrate and corresponding to each of the trenches may, in some embodiments, differ by less than approximately 10%, or more preferably by less than approximately 5%.

Please replace the paragraph beginning on pg. 8, line 15, with the following rewritten paragraph.

Consequently, the method as described herein may form a semiconductor topography including one or more trench isolation regions arranged within a semiconductor substrate and a plurality of layers arranged laterally adjacent to the trench isolation regions and upon the semiconductor substrate. In some embodiments, the plurality of layers may include a silicon nitride layer arranged above the semiconductor substrate and a silicon dioxide layer arranged upon the silicon nitride layer. In addition or alternatively, the upper surfaces of the trench isolation regions may be above the plurality of layers. For example, the upper surfaces of the trench isolation regions may be above the plurality of layers by an amount between approximately 300 angstroms and approximately 1000 angstroms. In some embodiments, the trench isolation regions may include two trench isolation regions spaced a first distance from each other. In addition, the trench isolation regions may include a third trench isolation region spaced a second distance from one of the two trench isolation regions. In such an embodiment, the second distance may be greater than the first distance. In addition, such an arrangement of isolation regions may not, in some embodiments, include any trench isolation regions interposed between the third trench isolation region and the one of the two trench isolation regions. In such an embodiment, the upper surfaces of the third trench isolation region may be farther above the plurality of layers than upper surfaces of the two trench isolation regions.

Please replace the paragraph beginning on pg. 13, line 8, with the following rewritten paragraph.

Stack of layers 20 may serve to protect portions of underlying layers and structures within semiconductor layer 10. For example, stack of layers 20 may protect portions of oxide 12 and semiconductor layer 10 from an etch process which may be used to form trenches 22, 24, and 26 within semiconductor layer 10. In a preferred embodiment, stack of layers 20 may include intervening layers of different etching characteristics. As such, intermediate layer 16, as shown in Fig. 1, may include different etch characteristics than upper layer 18 and lower layer 14. In some embodiments, upper layer 18 and

lower layer 14 may include similar etch characteristics. For example, upper layer 18 and lower layer 14 may include silicon nitride, while intermediate layer 16 may include silicon dioxide. In alternative embodiments, upper layer 18 and lower layer 14 may include different etch characteristics, and thus different materials. In addition or alternatively, stack of layers 20 may include intervening layers of different polishing characteristics. For example, upper layer 18 may include a polish stop material, such as silicon nitride. As such, lower layer 14 may include a material with similar polish stop characteristics. Intermediate layer 16, in such an embodiment, may include a material that polishes at a different rate than upper layer 18 and lower layer 14.

Please replace the paragraph beginning on pg. 19, line 8, with the following rewritten paragraph.

Consequently, structures 42, 44, and 46 may be formed within semiconductor topography 11. For example, in some embodiments, structures 42, 44, and 46 may include shallow trench isolation regions. Such structures may include step heights 48, which are the portion of structures 42, 44, and 48 residing above the upper surface of semiconductor layer 10. In some embodiments, step height 48 may be less than approximately 500 angstroms. More specifically, step height 48 may be between approximately 300 angstroms and 500 angstroms and in preferred embodiments approximately 400 angstroms. In an embodiment in which structures 42, 44, and 46 are isolation regions, such step heights of minimal thickness formed above semiconductor layer 10 may offer the additional benefit of preventing poly stringers from forming during subsequent processing, while insuring that the active regions of the semiconductor topography are sufficiently isolated. In a preferred embodiment, the average thicknesses of the each of step heights 48 corresponding to structures 42, 44, and 46 may differ by less than approximately 10%, or more preferably by less than approximately 5%. Since trenches 22, 24, and 26 are preferably formed with substantially level bases, the thickness variation between structures 42, 44, and 46 may differ by less than approximately 10% and in some embodiments, by less than approximately 5%. In some embodiments, the thickness variation between structures 42, 44, and 46 ~~by~~ differ by less than approximately 250 angstroms, and more preferably by less than approximately 200 angstroms.